CLAIMS

What is claimed is:

1. A bus bridge comprising:

a first serial bus interface, the first serial bus interface operable as a bus slave;

a target serial bus interface, the target serial bus interface operable as a bus master; and

apparatus coupling the first bus interface to the target serial bus interface, such that commands received by the first bus interface are capable of causing execution of commands by the target serial bus interface.

2. The bus bridge of Claim 1, wherein the target serial bus interface is a JTAG bus interface.

3. The bus bridge of Claim 2, wherein the first serial bus interface is an IIC bus interface.

4. The bus bridge of Claim 1, wherein the target serial bus interface is configured with a plurality of target serial bus ports, and further comprising selection logic, the selection logic coupled such that the first serial bus interface can designate which of the plurality of target serial bus ports of the target serial bus interface is to receive commands executed by the target serial bus interface.

5. The bus bridge of Claim 4, wherein the target serial bus interface is a JTAG bus interface.

6. The bus bridge of Claim 4, wherein the first serial bus interface is an IIC bus interface.

7. The bus bridge of Claim 6, further comprising a first FIFO buffer coupled to pass data from the first serial bus interface to the target serial bus interface, and a second FIFO buffer coupled to pass data from the second serial bus interface to the first serial bus interface.

8. The bus bridge of Claim 7, further comprising a status register coupled to be readable over the first serial bus interface, and wherein the status register has flags for detecting data in the first FIFO buffer and the second FIFO buffer.

9. A bus bridge comprising:

a first bus interface, the first bus interface operable as a bus slave;

apparatus for selecting a particular target bus port of a plurality of target serial bus ports, the apparatus for selecting a particular target bus port addressable through the first bus interface

apparatus for coupling to the particular target bus port, the apparatus for coupling operable as a bus master;

apparatus for transferring information between the first bus interface and the particular target bus port.

10. The bus bridge of Claim 9, wherein the plurality of target serial bus ports includes at least two JTAG bus ports.

11. The bus bridge of Claim 10, wherein the first serial bus interface is an IIC bus interface.

12. The bus bridge of Claim 11, wherein the apparatus coupling the first bus interface to the apparatus for coupling to a plurality of target serial bus ports comprises at least one FIFO.

13. The bus bridge of Claim 12, further comprising a bypass mechanism whereby data may be communicated between the first bus interface and apparatus for coupling to a plurality of target serial busses without using the FIFOS.

14. The bus bridge of Claim 13, implemented in an FPGA having an associated EEPROM for storing configuration code.

15. The bus bridge of Claim 14, wherein a serial bus of the target serial busses is coupled to the EEPROM, and wherein the EEPROM may be erased and written through the serial bus.

16. The bus bridge of Claim 15, wherein the serial bus of the target serial busses that is coupled to the EEPROM is also coupled to a configuration header.

17. The bus bridge of Claim 11, implemented in a bus bridge FPGA having an EEPROM associated therewith for storing configuration code, wherein a serial bus port of the target serial bus ports is coupled to the EEPROM associated with the bus bridge FPGA, and wherein the EEPROM associated with the bus bridge FPGA may be erased and written through the target serial bus port, thereby permitting modification of the bus bridge.